REMARKS

Claims 1, 9, 31, 53, 57, and 60 have been amended. Claims 5-6 and 54-56 have been canceled. No new claims have been added. Thus, claims 1-4, 7-28, 30-50, 52-53, 57-75, and 77 are pending.

Claims 1-15, 18, 21-23, 26-27, 30-37, 40, 43-45, 48-49, 52-65, 68, 73-75, and 77 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Leddige (U.S. Patent No. 6,587,912). Claims 28 and 50 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Leddige and Office Notice. Claims 16-17, 19, 20, 24-25, 38-39, 41-42, 46-47, 66-67, and 69-72 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Leddige and Halbert (U.S. Patent No. 6,625,687). These rejections are respectfully traversed.

Claim 1 recites, *inter alia*: "wherein said first and second receiver and driver pairs, said selector circuit, and said I/O device are disposed on a same integrated circuit."

Claim 9 recites, *inter alia*: "wherein ... said first and second receiver and driver pairs, said second data bus, and said device are located on a same integrated circuit."

Claim 31 recites, *inter alia*: "A memory module, comprising: at least one memory device, each one of said at least one memory device being disposed on an integrated circuit, and comprising: a memory; and a data transfer interface ... comprising: ... an interface circuit coupled to said first and second receiver and driver pairs and a second data bus, wherein said interface circuit is configured to receive data from said first receiver and selectively place said data on said second data bus, and

receive data on said second data bus and selectively place said data on said first data bus; wherein said second bus is coupled to said memory."

Claim 53 recites, *inter alia*: "a data transfer interface, disposed on an integrated circuit and comprising: ... a second data bus; a device, coupled to the second data bus; and an interface circuit coupled to said first and second receiver and driver pairs and a second data bus, wherein said interface circuit is configured to receive data on said first data bus and selectively place said data on said second data bus, and receive data on said second data bus and selectively place said data on said first data bus."

Claim 57 recites, *inter alia*: "wherein said first and second receivers, said first and second drivers, and said I/O device are disposed on a same integrated circuit."

Claim 60 recites, *inter alia*: "wherein said interface circuit, said second data bus, and said at least one device are disposed on a same integrated circuit."

Leddige discloses a memory system having a memory repeater hub (e.g., Fig. 3, 320) associated with a plurality of memory devices (e.g., Fig. 3, 301). Significantly, the memory repeater hub and the plurality of memory devices are discrete devices. Accordingly, Leddige fails to disclose or suggest the above quoted portions of the independent claims.

The Office Action additionally cites to Halbert. However, Halbert like Leddige also fails to disclose or suggest an integrated circuit having the features recited in the above quoted portions of the independent claims.

Accordingly, claims 1, 9, 31, 53, 57, and 60 are believed to be allowable over the prior art of record. The depending claims, (i.e., claims 2-4, 7-8, 10-28, 30, 32-50, 52,

58-59, 61-75, and 77) are also believed to be allowable for at least the same reason as the independent claims.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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